AMENDMENTS TO THE SPECIFICATION:

Please replace the Abstract of the Disclosure with the following rewritten Abstract which appears on a separate sheet.

Page 3, replace the paragraph beginning on line 14 with the following amended paragraph:

--The above-mentioned first group of hard-macros is necessary to be spaced away from adjacent hard-macros in order to ensure an area in which wires are to be arranged, and has a problem that wires ~~has~~ are to be arranged in a high density between hard-macros. Similarly, the above-mentioned second group of hard-macros is necessary to be spaced away from I/O pads in order to ensure an area in which wires are to be arranged.--

Page 5, replace the paragraph beginning on line 5 with the following amended paragraph:

--In one aspect of the present invention, and with reference to Figures 2-10 that are explained in more detail below, there is provided a hard-macro (1, 2, 100, 200, 300) arranged on a semiconductor chip (5) for constituting a part of a semiconductor integrated circuit, including at least one wire (11a-11f, 21a-21f, 204, 304) passing therethrough, wherein the wire (11a-11f, 21a-21f, 204, 304) is formed in the hard-macro (1, 2, 100, 200, 300) before the hard-macro (1, 2, 100, 200, 300) is arranged on the semiconductor chip (5), and the wire (11a-11f, 21a-21f, 204, 304) starts at a first outer edge (12, 22, 202, 302) of the hard-macro (1, 2, 100, 200, 300) and terminates at a

second outer edge (13, 14, 23, 24, 203, 303) of the hard-macro (1, 2, 100, 200, 300) intersecting with the first outer edge (12, 22, 202, 302).--

Page 5, replace the paragraph beginning on line 27 with the following amended paragraph:

--The hard-macro (1, 2, 100, 200, 300) may further ~~including~~ include a repeater ~~(100)~~ (110) inserted in the wire (11a-11f, 21a-21f, 204, 304).--

Page 5, replace the paragraph beginning on line 29 and bridging pages 5 and 6 with the following amended paragraph:

--The hard-macro (1, 2, 100, 200, 300) may include a plurality of wires (11a-11f, 21a-21f, 204, 304) passing therethrough, in which case, at least one of the wires (11a-11f, 21a-21f, 204, 304) may include a repeater (110) inserted therein.--

Page 6, replace the paragraph beginning on line 10 with the following amended paragraph:

--In another aspect of the present invention, there is provided a semiconductor integrated circuit including a hard-macro (1, 2, 100, 200, 300) arranged on a semiconductor chip (5) for constituting a part of the semiconductor integrated circuit, including at least one wire (11a-11f, 21a-21f, 204, 304) passing therethrough, wherein the wire (11a-11f, 21a-21f, 204, 304) is formed in the hard-macro (1, 2, 100, 200, 300) before the hard-macro (1, 2, 100, 200, 300) is arranged on the semiconductor chip

(5), and the wire (11a-11f, 21a-21f, 204, 304) starts at a first outer edge (12, 22, 202, 302) of the hard-macro (1, 2, 100, 200, 300) and terminates at a second outer edge (13, 14, 23, 24, 203, 303) of the hard-macro (1, 2, 100, 200, 300) intersecting with the first outer edge.--

Page 6, replace the paragraph beginning on line 22 and bridging pages 6 and 7 with the following amended paragraph:

--In still another aspect of the present invention, there is provided a floor-planner (4) including a device (42) for analyzing a floor-plan of a semiconductor integrated circuit including a hard-macro (1, 2, 100, 200, 300) arranged on a semiconductor chip (5) for constituting a part of the semiconductor integrated circuit which hard-macro (1, 2, 100, 200, 300) includes at least one wire (11a-11f, 21a-21f, 204, 304) passing therethrough, wherein the wire (11a-11f, 21a-21f, 204, 304) is formed in the hard-macro (1, 2, 100, 200, 300) before the hard-macro (1, 2, 100, 200, 300) is arranged on the semiconductor chip (5), and the wire (11a-11f, 21a-21f, 204, 304) starts at a first outer edge (12, 22, 202, 302) of the hard-macro (1, 2, 100, 200, 300) and terminates at a second outer edge (13, 14, 23, 24, 203, 303) of the hard-macro (1, 2, 100, 200, 300) intersecting with the first outer edge.--

Page 7, replace the paragraph beginning on line 7 with the following amended paragraph:

--In still another aspect of the present invention, there is provided a floor-planner (4) including a device (42) for analyzing a floor-plan of a semiconductor integrated circuit including a hard-macro (1, 2, 100, 200, 300) arranged on a semiconductor chip (5) for constituting a part of the semiconductor integrated circuit which hard-macro (1, 2, 100, 200, 300) includes at least one wire (11a-11f, 21a-21f, 204, 304) passing therethrough, wherein the wire (11a-11f, 21a-21f, 204, 304) is formed in the hard-macro (1, 2, 100, 200, 300) before the hard-macro (1, 2, 100, 200, 300) is arranged on the semiconductor chip (5), and the wire (11a-11f, 21a-21f, 204, 304) starts at a first outer edge (12, 22, 202, 302) of the hard-macro (1, 2, 100, 200, 300) and terminates at a second outer edge (13, 14, 23, 24, 203, 303) of the hard-macro (1, 2, 100, 200, 300) intersecting with the first outer edge.--

Page 8, replace the paragraph beginning on line 16 with the following amended paragraph:

--In the hard-macro in accordance with the present invention, the wire passing through the hard-macro is designed to extend from a first outer edge of the hard-macro to a second outer edge of the hard-macro intersecting with the first outer edge, when viewed perpendicularly. Hence, a wire which is necessary to extend between the first and second outer edges of

the hard-macro can be made by using the wire passing through the hard-macro. Thus, it is possible to minimize a space between the hard-macro in accordance with the present invention and other hard-macros located in the vicinity of the first or second outer edge of the hard-macro.--